APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,092	12/28/2001	James S. Burns	42390P12492	2392

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Leo V. Novakoski
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, CA 90025-1026

CHEN, TSE W

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)
Office Action Summary	10/041,092	BURNS ET AL.
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

À SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>20 December 2005</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-21 and 23-30* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-21 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

U.S. Patent and Trademark Office

PTOL-326 (Rev. 7-05)   Office Action Summary   Part of Paper No./Mail Date 02062006

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on December 20, 2005 has been entered.

2.   Claims 1, 3-5, 7-21, and 23-30 are presented for examination. Applicant has canceled

claims 2, 6, and 22.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
> in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
> patent by another filed in the United States before the invention by the applicant for patent, except that an
> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
> subsection of an application filed in the United States only if the international application designated the United
> States and was published under Article 21(2) of such treaty in the English language.

4.   Claims 1, 3, 11-12, 19-20, 23-30 are rejected under 35 U.S.C. 102(e) as being anticipated

by Soltis, Jr. et al., US Patent 6651176, hereinafter Soltis.

5.   In re claim 1, Soltis discloses a system [100] comprising:

- An execution pipeline [116].

- A power delivery unit [associated with inherent clock gating circuit to control clock

    capacity with the lp-bits; pipelined processor powered according to clock capacity] to

    provide power to the execution pipeline at a specified operating point [col.4, ll.40-56;

col.5, 1.66 – col.6, 1.62; col.7, 11.14-56; full or low power state as related to bleed rate],

wherein the power delivery unit includes a clock gating circuit [inherently, some clock

gating circuit in the broadest interpretation is needed to control clock capacity with the

lp-bits, requiring plural clock gate units for pipeline with multiple executing stage units]

to control power delivery to one or more units of the execution pipeline [col.2, 1.66 –

col.3, 1.40; col.4, 11.9-67; clock capacity related to lp-bits].

- A digital throttle [power dissipation controller 118] to estimate a power state [capacity

  322], responsive to activity of the execution pipeline and the specified operating point,

  and to trigger a change in the operating point, responsive to the estimated power state

  reaching a first threshold [363] [col.4, 11.9-17, 11.40-56; col.5, 1.66 – col.6, 1.62; col.7,

  11.14-56; col.8, 11.25-36; switch to low power state if capacity as determined by first

  power dissipation at full power state exceeds threshold].

6.   As to claim 3, Soltis discloses the system wherein the digital throttle comprises an

activity monitor to estimate an activity level [first power dissipation] responsive to a signal [valid

instructions] from the clock gating circuit, the activity monitor including a scaling unit [issue

weight] to adjust the estimated activity level, responsive to the current operating state [col.2, 1.66

– col.3, 1.40; col.4, 11.9-67].

7.   In re claim 11, Soltis and Huang discloses each and every limitation of the claim as

discussed above in reference to claims 1 and 3.

8.   As to claim 12, Soltis discloses the processor wherein the scaling unit includes a look-up

table [119] and a multiplier, the look-up table to provide a scale factor [constants; i.e., weights]

[col.4, 11.57-67] to the multiplier, responsive to the operating point of the processor [col.4, 11.9-

25].

9.   In re claim 19, Soltis discloses each and every limitation as discussed above in reference

to claims 1 and 11. Soltis discloses the processor; therefore, Soltis discloses the method of

operating the processor. Additionally, Soltis discloses monitoring activity states for pipeline

units of the processor [col.2, 1.66 – col.3, 1.40; col.4, 11.9-67].

10.   As to claim 20, Soltis discloses each and every limitation of the claim as discussed above

in reference to claim 19. Additionally, Soltis discloses normalizing the scaled activity level

relative to a first threshold and accumulating the normalized, scaled activity level for a series of

clock intervals [col.2, 1.66 – col.3, 1.40; col.4, 11.9-67; fig.8; normalizing to target].

11.   As to claims 23-24, Soltis discloses the method wherein adjusting the operating point of

the processor comprises adjusting a frequency and voltage of the clock signal [col.2, 1.66—col.3,

1.40].

12.   As to claim 25, Soltis discloses the method wherein estimating the activity level

comprises adding a first or a second weight value to a sum, responsive to a pipeline unit being in

a first or a second activity state, respectively and scaling the sum by a factor associated with the

current operating point [col.2, 1.66 – col.3, 1.40; col.4, 11.9-67; col.7, 1.14 – col.8, 1.47].

13.   As to claim 26, Soltis discloses the method wherein estimating the activity level

comprises adding a weight to the sum to represent pipeline units that operate in a single activity

state [col.2, 1.66 – col.3, 1.40].

14.   In re claim 27, Soltis discloses each and every limitation of the claim as discussed above

in reference to claim 1, 11 and 19. Additionally, Soltis discloses a memory system to store

instructions for execution [instruction cache 114].

15.   As to claim 28, Soltis discloses the computer system wherein each gate unit indicates a

first or second activity state for a unit of the execution pipeline, according to the unit's being

active or inactive in a clock interval [col.6, ll.16-62; tagging of lp-bits].

16.   As to claims 29 and 30, Soltis discloses each and every limitation as discussed above in

reference to claim 25.

Claim Rejections - 35 USC § 103

17.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18.   Claims 4 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soltis as

applied to claim 3 above, and further in view of Dunstan et al., US Patent 5694607, hereinafter

Dunstan.

19.   In re claims 4 and 7, Soltis discloses each and every limitation of the claim as discussed

above. In particular, Soltis discloses the system wherein the scaling unit includes a look-up table

[119] to store scaling factors [constants; i.e., weights] [col.4, ll.57-67] and a multiplier to

multiply the estimated activity level by the scaling factor associated with the current operating

point [col.4, ll.9-25]. Soltis did not disclose explicitly multiple operating states.

20.   Dunstan discloses a look-up table [70] to store values for a plurality of operating states

[configurations] [col.7, ll.39-65].

21.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Dunstan and Soltis before him at the time the invention was made, to use the look-up table taught

by Dunstan for the system disclosed by Soltis in order to provide the system wherein the scaling

unit includes a look-up table to store scaling factors for a plurality of operating points. One of

ordinary skill in the art would have been motivated to make such a combination as it provides a

way to track and control power consumption in a multiple operating state system [Dunstan: col.1,

l.9 – col.2, l.51].

22.   As to claim 8, Soltis discloses the system comprising a conversion circuit [part of 118] to

determine a power state [capacity] from the adjusted activity level [col.4, ll.9-17, ll.40-56; col.5,

l.66 – col.6, l.62; col.7, ll.14-56; col.8, ll.25-36].

23.   As to claim 9, it is well known in the art to store values [e.g., comparative differences] in

an accumulator in order to indicate status.

24.   Claims 5 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soltis

as applied to claims 3 and 11 above, and further in view of Niegel et al., US Patent 6512757,

hereinafter Niegel.

25.   In re claim 5, Soltis and Huang disclose each and every limitation of the claim as

discussed above. Soltis did not discuss weight units associated with the units of the pipeline.

26.   Niegel discloses a system wherein a monitor unit comprises a plurality of weight units,

each weight unit being associated with one of the units of execution pipeline and an adder to

receive a first or second value from each weight unit [col.2, l.57 – col.2, l.31].

27.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Niegel and Soltis before him at the time the invention was made, to use the weight units taught

by Niegel for the system disclosed by Soltis in order to provide the system wherein the monitor

unit comprises a plurality of weight units, each weight unit being associated with one of the units

of the execution pipeline and an adder to receive a first or second value from each weight unit,

responsive to the signal from the clock gating circuit.. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to process a plurality of data channels at reduced hardware costs, while maintaining a high processing speed and short time delay [Niegel: col.1, 1.13 – col.2, 1.41].

28.   As to claim 16, Niegel and Soltis disclose each and every limitation of the claim as discussed above in reference to claim 5.

29.   As to claim 17, Niegel and Soltis disclose each and every limitation of the claim as discussed above in reference to claim 16. Niegel and Soltis did not disclose explicitly monitoring status signals provided by the gate units.

30.   It would have been obvious to one with ordinary skill in the art to monitor the activity states by monitoring the status signals provided by gate units associated with the pipeline units of the processor as the monitoring of the status signals is well-known in the art and suitable for use in the system disclosed by Niegel and Soltis. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to gauge the status of activity in the pipeline.

31.   As to claim 18, Niegel and Soltis disclose each and every limitation of the claim as discussed above in reference to claims 16 and 17.

32.   Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dunstan and Soltis as applied to claim 9 above, and further in view of Yochai et al., US Patent 6721870, hereinafter Yochai.

33.   Dunstan and Soltis disclose each and every limitation as discussed above in reference to claim 9. Dunstan and Soltis did not discuss scaling the threshold level.

34.   Yochai discloses a system wherein a conversion unit scales the threshold level responsive to the current operating point [col.9, l.65 – col.10, l.50].

35.   It would have been obvious to one of ordinary skill in the art, having the teachings of Yochai, Dunstan and Soltis before him at the time the invention was made, to use the conversion unit taught by Yochai for the system disclosed by Dunstan and Soltis in order to provide the system wherein the conversion unit scales the threshold level responsive to the current operating point. One of ordinary skill in the art would have been motivated to make such a combination as it provides an efficient way to prefetch instructions or data [Yochai: col.1, l.27 – col.2, l.11].

36.   Claims 13-15, 19-21 and 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soltis, as applied to claims 11-12, 14 and 19 above.

37.   Soltis discloses each and every limitation of the claim as discussed above. Soltis did not disclose explicitly the following prior art elements from previous Official Notice.

38.   As to claim 13, it is well known in the art to specify an operating state [e.g., low or full power] by a voltage and a frequency [decreasing clock frequency decreases power consumption] in order to differentiate an operating state.

39.   As to claim 14, it is well known in the art to increment values [e.g., comparative differences] in an accumulator in order to indicate some status.

40.   As to claim 15, it is well known in the art to have multiple threshold comparisons in order to transition to different states.

41.   As to claim 21, it is well known in the art to monitor the activity states by monitoring the status signals provided by gate units associated with the pipeline units of the processor in order to gauge the status of activity in the pipeline.

Response to Arguments

42.   Applicant's arguments dated December 20, 2005 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
February 6, 2006

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100